PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 :
H01L 23/28, 23/48, 29/44
H01L 29/52, 29/54, 29/60

A1

(11) International Publication Number: WO 87/ 04008

(43) International Publication Date: 2 July 1987 (02.07.87)

(21) International Application Number: PCT/US86/01883

(22) International Filing Date: 15 September 1986 (15.09.86)

(31) Priority Application Number: 810,452

(32) Priority Date: 18 December 1985 (18.12.85)

(33) Priority Country: US

(71) Applicant: MOTOROLA, INC. [US/US]; 1303 E. Algonquin Road, Schaumburg, IL 60196 (US).

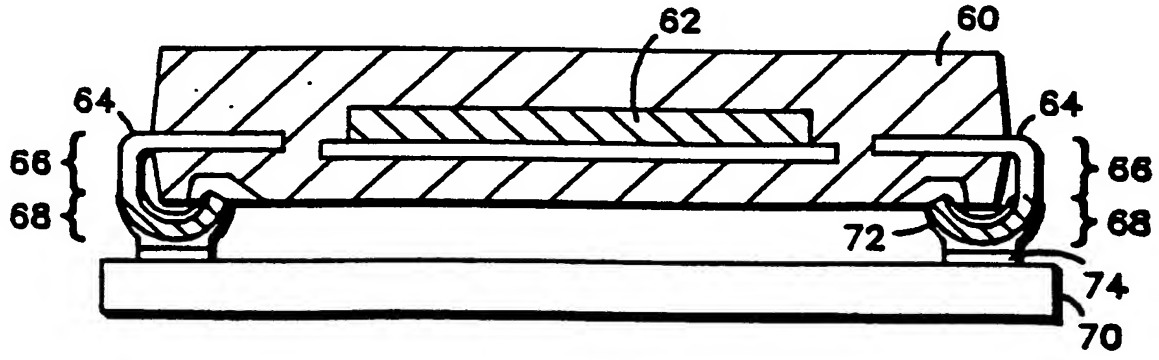
(72) Inventor: LIN, Paul, T. ; 9813 Mandeville Circle, Austin, TX 78750 (US).

(74) Agents: MOSSMAN, David, L. et al.; Motorola, Inc., Patent Department - Suite 300K, 4250 E. Camelback Road, Phoenix, AZ 85018 (US).

(81) Designated States: DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, NL (European patent).

Published
With international search report.
With amended claims.

(54) Title: LEAD FINISHING FOR A SURFACE MOUNT PACKAGE



(57) Abstract

A surface mount package (60) having a plurality of exterior package leads (64) with a dual finished surface (66, 68). The lower part of the lead which is to be bonded to a bonding pad (74) of a substrate (70) such as a printed circuit board is provided with a solder-wettable surface (68) which extends only part-way up the length of the lead (64) to meet with a non-wettable surface region (66). Alternately, or in addition thereto, the upper portions of the leads (64) may be coated with a chemical, plastic or other solder- phobic composition (84) to provide the non-wettable surface region (66). Bonds made using such leads (64) are stronger and more reliable because of the affinity of the solder (72) for the lead (64) at the contact area (74) and the aversion of the solder (72) to wick up the lead into the non-wettable area (66) of the lead (64) nearer the package (60) and thus draw solder (72) away from the bonding area (74). The configuration of the solder bond is easily and quickly adjusted by controlling the area or depth of the solder coated region (68) on only the lower portion of the leads (64) of the surface mountable integrated circuit package (60).

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**FR**	France	**ML**	Mali
AU	Australia	**GA**	Gabon	**MR**	Mauritania
BB	Barbados	**GB**	United Kingdom	**MW**	Malawi
BE	Belgium	**HU**	Hungary	**NL**	Netherlands
BG	Bulgaria	**IT**	Italy	**NO**	Norway
BJ	Benin	**JP**	Japan	**RO**	Romania
BR	Brazil	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SN**	Senegal
CH	Switzerland	**LI**	Liechtenstein	**SU**	Soviet Union
CM	Cameroon	**LK**	Sri Lanka	**TD**	Chad
DE	Germany, Federal Republic of	**LU**	Luxembourg	**TG**	Togo
DK	Denmark	**MC**	Monaco	**US**	United States of America
FI	Finland	**MG**	Madagascar		

LEAD FINISHING FOR A SURFACE MOUNT PACKAGE

Field of the Invention

This invention relates to integrated circuit packages and more particularly relates to surface mountable integrated circuit packages and the solder bonding thereof.

Background of the Invention

Integrated circuits were early encased in dual-in-line packages (DIPs), which are small, elongated plastic boxes with the exterior leads coming out on either side of the box and turning down in two parallel rows, one along each side of the package. DIPs are mounted into corresponding holes in a printed circuit board that have been plated through and to which the DIPs are soldered to make electrical and mechanical connection.

As integrated circuits became smaller and more complex, the number of leads coming out of the package increased, even though the package size remained the same or decreased. One solution to this problem was the flat, plastic leaded chip carrier (PLCC), which typically is a small, flat, square package having the leads coming out and formed around each of the four edges of the package. PLCCs are typically mounted in sockets with contacts that mate with the leads on the PLCCs.

More recently PLCCs have been surface mounted directly on the corresponding pattern of electrical contact pads on a printed circuit board. Surface mounting of parts has gained widespread interest of late because of the ease with which the parts can be picked up and placed on the printed circuit board in contrast to a through-hole package which must be much more precisely aligned. Not only may a printed circuit board be more easily populated with ICs, but they may also be more easily removed. In addition, it is possible to achieve a higher density of ICs on a printed circuit board with surface

mount packages. Also, the leads on the packages to be surface mounted are often much shorter and better protected than leads that are mounted through holes in the printed circuit board so that there is less danger of damage to the leads during handling of surface mountable packages. The leads on surface-mounted packages such as PLCCs, quad packs or DIPs tend to be of one of three types: J-lead, butt joint and gull wing. J-Leads come out from the side of the package body and turn down and curl under and into the package bottom. The mounting surface for a J-lead is the bottom of the curl. Butt joint leads come out from the side of the package body and turn down and meet the mounting substrate head-on and perpendicular to the mounting surface. Finally, gull wing leads come out from the side of the package body and turn down and then turn out away from the package parallel to the mounting substrate surface.

Typically, for all of the surface mount lead forms, both the leads and the bonding pads on the mounting substrate, such as a printed circuit board, are plated or coated with tin or solder. A solder mask for the printed circuit (PC) board must be defined and generated, after which the solder paste must be applied to the PC board which requires an alignment step of the mask. The actual application of solder paste is typically done using a stencil process or a screen process, as in silk screen printing, both of which involve many variables and can be complex. The leads of the surface mount devices are also plated or coated with tin or solder in some fashion and then picked up and positioned onto the PC board, which has two patterns thereon, the PC artwork and the solder mask artwork. This positioning constitutes a second alignment step. Finally, the solder undergoes reflow to make the surface joint by either a vapor phase or an infrared (IR) treatment. Often, the leads do not have tin or solder on their ends which produces weak bonds as will be described later.

The solder reflow step to make the mechanical and electrical bond of the lead to the substrated bonding pad can run afoul in a number of different ways. For example, FIG. 1 demonstrates the appropriate bond 10 of J-lead 12 of package

14 to bonding pad 16 of substrate 18 which is difficult to achieve in practice. If as in FIG. 2, the solder 20 does not properly wet the plating on lead 22 of package 24, dewetting occurs and the bond area of lead 22 to bonding pad 26 of substrate 28 shrinks undesirably to give a bond that is weak both mechanically and electrically. This solder dewetting problem typically occurs in cases where the leads have been solder plated. The typical solution includes additional fusing or reflow steps for the uncoated or thin lead ends, where this is a particular problem for gull wing and butt joint leads.

An opposite effect may also commonly occur as shown in FIG. 3 where the solder paste 30 sufficiently wets the lead 32 of package 34 but tends to wick up the lead 32 rather than stay near bonding pad 36 of substrate 38, again reducing the bonding area forming a weak mechanical and electrical bond. The wicking problem tends to occur if the leads are wave soldered or solder dipped. Another problem with the wave soldering or solder dipping of the entire lead is that only a limited solder coating thickness may be applied and that often the coating on the lead corners of the resulting bond is too thin. This is particularly a problem with J-leads.

Proposed solutions to the dewetting and wicking problems of surface mount leads include using physical solder dams around the bonding pads of the substrate to shape the bond as it is being formed, and to use a clad or sandwich lead as shown in FIG. 4. Lead 40 of package 42 is made up of three layers, the interior layer 44 which is the lead metal and the bulk of lead 40, an outer wettable material layer 46 such as nickel and an inner non-wettable material layer 48 such as an aluminum bronze. While such a structure helps alleviate the wicking problem up the interior portion of the lead, wicking of solder 50 may still occur on the outer layer 46, again reducing the bonding area of lead 40 to bonding pad 52 on substrate 54. Additionally, such a lead 40 is much more complex in structure and therefor more costly than the standard plated lead.

One problem with the tin plating that is sometimes

used on the leads of the surface mountable packages is that tin whiskers or intermetallic lines often form between leads over a period of time which cause leakage problems. Another problem with tin or solder plated leads is that, in general, the leads have uncoated, bare metal ends, because the parts are plated in strip form and cut to size to form the leads. Uncoated, bare metal ends are a problem, particularly in the butt joint form of surface mount devices because the end of the lead is thus not wettable by solder and voids under the lead end tend to form which compromise the electrical and mechanical integrity of the bond.

It would be an advance in the art if an inexpensive lead for surface mountable packages could be devised which would avoid the dewetting and wicking problems described.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a lead for surface mountable packages which is solder wettable but which does not permit the solder to wick up the lead during a bonding operation.

Another object of the invention is to provide a surface mountable package lead that is inexpensive and readily manufacturable.

Yet another object of the present invention is to provide a lead for surface mountable packages that avoids thin solder coatings.

Still another object of the invention is to provide a butt joint surface mountable package having the above-noted features and wherein the ends of the leads are also made solder-wettable.

In carrying out these and other objects of the invention, there is provided, in one form, a surface mountable integrated circuit package having a package body and a plurality of exterior leads depending therefrom in which only the upper portions of the exterior leads adjacent the package body are provided with a non-solder-wettable surface.

Brief Description of the Drawings

FIG. 1 is a cross-section of a portion of a surface mountable integrated circuit (IC) package of the prior art illustrating a proper solder bond;

FIG. 2 is a cross-sectional illustration of a portion of a surface mounted IC package having a solder bond that is unacceptable due to a problem with dewetting of the lead;

FIG. 3 is a cross-sectional illustration of a portion of a surface mountable IC package having a solder bond that is improperly formed due to wicking of the solder up the wettable lead;

FIG. 4 is another cross-sectional illustration of a portion of a surface mountable IC package, showing a prior art solution to part of the bonding problems;

FIG. 5 is a cross-sectional drawing of a portion of a surface mountable IC package which illustrates the leads of the present invention;

FIG. 6 is a cross-sectional illustration of another embodiment of the invention revealing how the surface of the upper portions of the exterior leads may be provided with a chemical coating to render them non-wettable by solder or flux; and

FIG. 7 is another cross-section of an alternate embodiment illustrating a surface mountable DIP where the entire package body as well as the upper portions of the exterior leads have been coated.

Detailed Description of the Invention

The prior art forms of leads to surface mountable IC packages have already been discussed, but it should be remembered that the correct and proper solder bond 10 shown in FIG. 1 is, in actual practice, difficult to achieve due to the problems of solder dewetting seen in FIG. 2 and solder wicking seen in FIG. 3. It should be noted that the term "solder" as used herein includes flux, solder paste and all other means of

forming a metal-to-metal electrically conductive contact by means of a flowable material that may be changed in some manner to form at least a hard bond.

The prior art solution to the surface mount problems using double clad lead 40 of FIG. 4 is only a partial solution to these problems in that while dewetting does not happen on outside layer 46, a wicking problem of the solder 50 up the lead 40 may still occur.

Shown in FIG. 5 is a surface mountable IC package 60 housing an integrated circuit chip 62, having a plurality of partially finished J-leads 64 of the present invention. While J-leads are illustrated, it will be understood that butt joint and gull wing leads also suffer from the problems described above which may also be solved by the structure of the present invention. J-leads have been chosen to illustrate the invention since the dewetting and wicking problems with solder are particularly pronounced with J-leads.

J-Leads 64 have two portions, one of which is an upper or dewetting portion 66 which may comprise the bare lead metal or the lead which has been entirely plated with a dewetting substance such as a lead/tin solder composition where the proportion by weight of lead to tin is 90/10 or more. There is an apparent inconsistency in calling the upper part of lead 64 "non-solder-wettable" when in fact it is plated with a lead/tin formulation. It should be noted that the plating substance while indeed a formulation of lead and tin and therefore a solder in the broadest sense, has such a high lead content that it may be considered "non-wettable" by the solder formulations required to be used to obtain the acceptable electrical and physical bond of a lead 64 to a bonding pad 74.

On the lower portion of leads 64 is a solder wettable surface 68 which extends only part-way up the lead 64. In one form of the invention, solder wettable surface 68 covers only the lower half or less of lead 64. The solder wettable surface 68 may be a metal surface or a plated surface that is wettable by solder or may be a surface that already has a thin solder coating thereon. In a more particular embodiment, the region 68 is a solder coating having a composition with a lead

to tin weight ratio of 63/37 or less, such as 60/40, which is applied by wave soldering the lower ends of leads 64 or by dipping just the ends of leads 64 into a solder paste or molten solder bath. Ordinarily this procedure would give a wicking problem, but since the solder-philic region is only part-way up the length of the lead and meets with a solder-phobic region, a proper bond may be formed without the wicking problem. It is anticipated that the leads of the present invention could be assembled in a variety of ways including covering the entire lead 64 with a solder wettable surface 68 and then applying a non-wettable surface, coating or plating 66 on the upper half or more of the lead. Alternately, lead 64 could be partially covered with a non-wettable surface 66 and partially covered with a wettable surface 68 in any appropriate sequence.

The exact proportion of lead 64 covered by solder coated area 68 is not important. In most cases, solder coated area 68 should cover an area equal to and slightly more than that area of lead 64 needed to obtain a good or ideal solder bond 72 to the substrate 70. One will have to optimize where the wettable/non-wettable interface is to be as a function of pad size and shape on the substrate. For most surface mountable packages 60, solder coated area 68 may be at least the lower half of lead 64.

The mounting of IC package 60 onto printed circuit (PC) board substrate 70 is conducted in the customary fashion. Solder 72 in the form of a paste or coating is placed on the the bonding pads 74 of the PC board substrate 70. Leads 64 are then aligned to correspond to the pattern of bonding pads 74 on PC board 70 and a solder reflow operation is performed to create the solder bonds. Since the lower portion 68 of the leads is solder wettable, a good bond forms, particularly because the solder 72 cannot wick up past the boundary of coated and wettable region 68; it being repelled by upper non-wettable region 66.

Thus, the leads 64 of the present invention avoid thin solder coatings thereon due to the presence of solder wettable region 68. Since the lead ends are provided with solder paste

wettable surfaces 68, the surface joints are optimized to only those areas of lead 64 and bonding pad 74 actually involved in the solder bond. Because the bonding structure and method of this invention do not involve tin plating, tin whisker leakage and tin intermetallic formation problems are avoided.

It should also be noted that the substrate level solder joint configuration can be controlled by controlling the depth of the solder dip onto the leads, that is the wettable surface area 68. If more solder is needed for a proper bond, the leads 64 may be dipped or wave soldered somewhat deeper, or if less solder 72 is needed on the leads 64, the package should not be dipped or wave soldered as deeply. In other words, adjustments may be made to the solder application step quickly and easily. In addition, burn-in can be performed between the step of solder plating of the entire lead 64 to form non-wettable upper region 66 and a solder dipping step to form wettable area 68 in order to minimize lead surface oxidation.

Shown in FIG. 6 is an alternate embodiment of the invention in the form of PLCC 76 having a package body 78 bearing an integrated circuit chip 80, from which a plurality of exterior J-leads 82 depend. The upper non-solder-wettable surface of the J-leads 82 is provided by a non-solder-wettable coating 84 which as illustrated also covers part of the package body 78. The coating 84 may be of any suitable material as long as it adheres to the package body 78 and exterior leads 82 and is solder-phobic. Any of a number of chemical coating substances would be suitable, and an example of a suitable material is an ultraviolet (UV) light-curable polymer plastic. The coating 84 may be applied simply by inverting the PLCC 76 and dipping it top down into the liquid chemical and then curing the chemical by the appropriate mechanism. It may be readily seen that coating 84, not being solder-wettable, will effectively prevent solder from wicking up lead 82 in a solder reflow operation.

Coating 84 provides the additional advantage of sealing any stress cracks 86 that may be present at the point the J-leads 82 project from the package body 78, which is a common problem with PLCCs. Stress cracks 86 are undesirable because

they provide a means whereby moisture and other contaminants may enter package body 78 and damage chip 80.

As in the other embodiments of the invention, exterior leads 82 have a lower solder coated portion 88 which is positioned over bonding pad 90 of substrate 92 and processed through a reflow operation to form solder bonds 94 as described previously.

FIG. 7 illustrates still another form of the invention; in this case a DIP 96 having a package body 98 and a plurality of exterior butt joint leads 100 designed to correspond with the bonding pads 102 on substrate 104. As in the case of the PLCC 76 of FIG. 6, a coating 106 is present to provide the upper non-wettable surface to exterior leads 100. However, in this case, package body 98 is entirely sealed in coating 106 to provide further protection to the package body 98 and the integrated circuit therein. Of course, the DIP 96 additionally has the characteristics of the PLCC 76 of FIG. 6, including the sealing of any microcracks that may be present.

CLAIMS

I Claim:

1. A surface mountable integrated circuit package comprising a package body and a plurality of exterior leads extending therefrom, wherein the leads have proximal ends adjacent to the package body and distal ends away from the package body and in which only the proximal ends of the exterior leads adjacent the package body are provided with a non-solder-wettable surface.

2. The surface mountable integrated circuit package of claim 1 in which the non-solder-wettable surface is a surface provided with a lead-heavy formulation having a lead to tin ration of at least 90/10.

3. The surface mountable integrated circuit package of claim 1 in which the non-solder-wettable surface is a coating covering the exterior leads as they project from the package body as well as only the proximal ends of the exterior leads.

4. The surface mountable integrated circuit package of claim 3 in which the coating is an ultraviolet curable plastic.

5. A surface mountable integrated circuit package comprising a package body and a plurality of exterior leads depending therefrom, wherein the leads have upper portions adjacent to the package body and lower portions away from the package body in which only the upper portions of the exterior leads adjacent the package body are provided with a non-solder-wettable surface, wherein the non-solder-wettable surface is different from the package body.

6. The surface mountable integrated circuit package of claim 5 in which the non-solder-wettable surface is a surface provided with a lead-heavy formulation having a lead to tin ratio of at least 90/10.

7. The surface mountable integrated circuit package of claim 5 in which the non-solder-wettable surface is a coating covering the exterior leads as they project from the package body as well as only an upper portion of the exterior leads.

8. A surface mountable integrated circuit package comprising a package body and a plurality of exterior leads extending therefrom, each lead having a proximal end connected to the package body and a distal end to be surface mounted to a substrate and a solder-coatable surface on only the distal ends thereof.

9. The surface mountable integrated circuit package of claim 8 in which the proximal ends of the exterior leads are provided with a non-wettable surface different from the package body and the distal ends of the exterior leads are provided with a solder coated surface by a process selected from the group consisting of wave soldering, solder paste dipping and molten solder dipping.

10. The surface mountable integrated circuit package of claim 8 in which the proximal ends of the exterior leads are provided with a non-wettable solder surface having a lead to tin ratio of at least 90/10 and in which the distal ends of the exterior leads are provided with a solder coated surface having a lead to tin ratio of less than or equal to 63/37.

AMENDED CLAIMS
[received by the International Bureau on 24 February 1987 (24.02.87); original claims 1,2,5, and 8 amended; other claims unchanged (2 pages)]

1. (Amended) A surface mountable integrated circuit package comprising a package body and a plurality of exterior leads extending therefrom, wherein the leads have proximal ends adjacent to the package body and distal ends away from the package body and in which only the proximal ends of the exterior leads adjacent the package body are each provided with an individual non-solder-wettable surface.

2. (Amended) The surface mountable integrated circuit package of claim 1 in which the non-solder-wettable surface is a surface provided with a lead-heavy formulation having a lead to tin ratio of at least 90/10.

3. The surface mountable integrated circuit package of claim 1 in which the non-solder-wettable surface is a coating covering the exterior leads as they project from the package body as well as only the proximal ends of the exterior leads.

4. The surface mountable integrated circuit package of claim 3 in which the coating is an ultraviolet curable plastic.

5. (Amended) A surface mountable integrated circuit package comprising a package body and a plurality of exterior leads depending therefrom, wherein the leads have upper portions adjacent to the package body and lower portions away from the package body in which only the upper portions of the exterior leads adjacent the package body are each provided with an individual non-solder-wettable surface, wherein the non-solder-wettable surface is different from the plastic body.

6. The surface mountable integrated circuit package of claim 5 in which the non-solder-wettable surface is a surface provided with a lead-heavy formulation having a lead to tin ration of at least 90/10.

7. The surface mountable integrated circuit package of claim 5 in which the non-solder-wettable surface is a coating covering the exterior leads as they project from the package body as well as only an upper portion of the exterior leads.

8. (Amended) A surface mountable integrated circuit package comprising a package body and a plurality of exterior leads extending therefrom, each lead having a proximal end connected to the package body and a distal end to be surface mounted to a substrate and an individual solder-coatable surface on only the distal ends thereof.

9. (Amended) The surface mountable integrated circuit package of claim 8 in which the proximal ends of the exterior leads are each provided with an individual non-wettable surface different from the package body and the distal ends of the exterior leads are each provided with an individual solder coated surface by a process selected from the group consisting of wave soldering, solder paste dipping and molten solder dipping.

10. The surface mountable integrated circuit package of claim 8 in which the proximal ends of the exterior leads are provided with a non-wettable solder surface having a lead to tin ratio of at least 90/10 and in which the distal ends of the exterior leads are provided with a solder coated surface having a lead to tin ratio of less than or equal to 63/37.

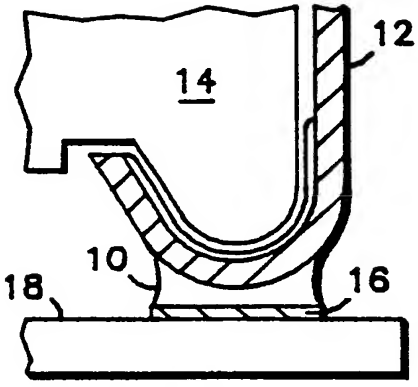


FIG. 1
-PRIOR ART-

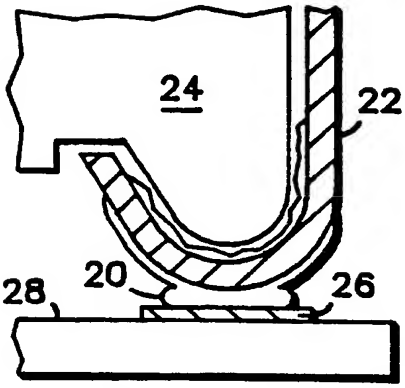


FIG. 2
-PRIOR ART-

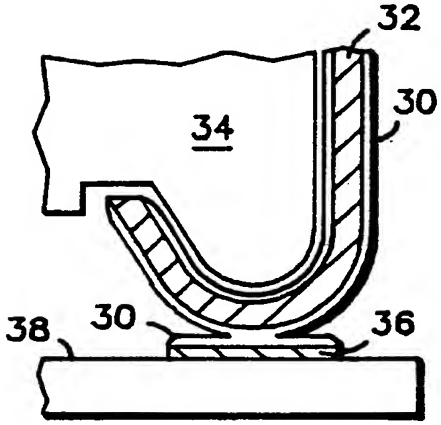


FIG. 3
-PRIOR ART-

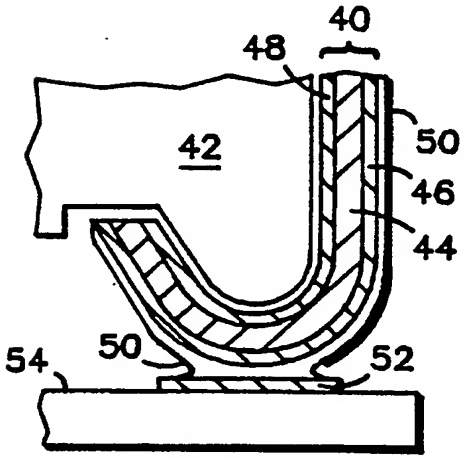
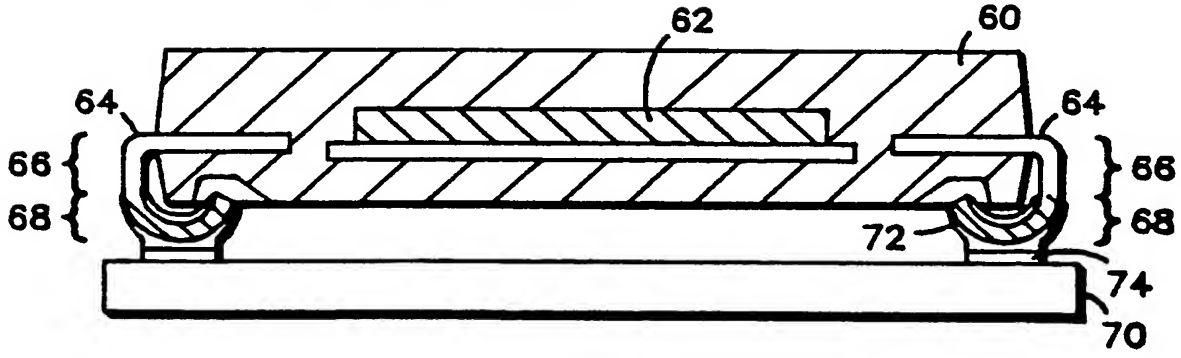


FIG. 4
-PRIOR ART-

FIG. 5



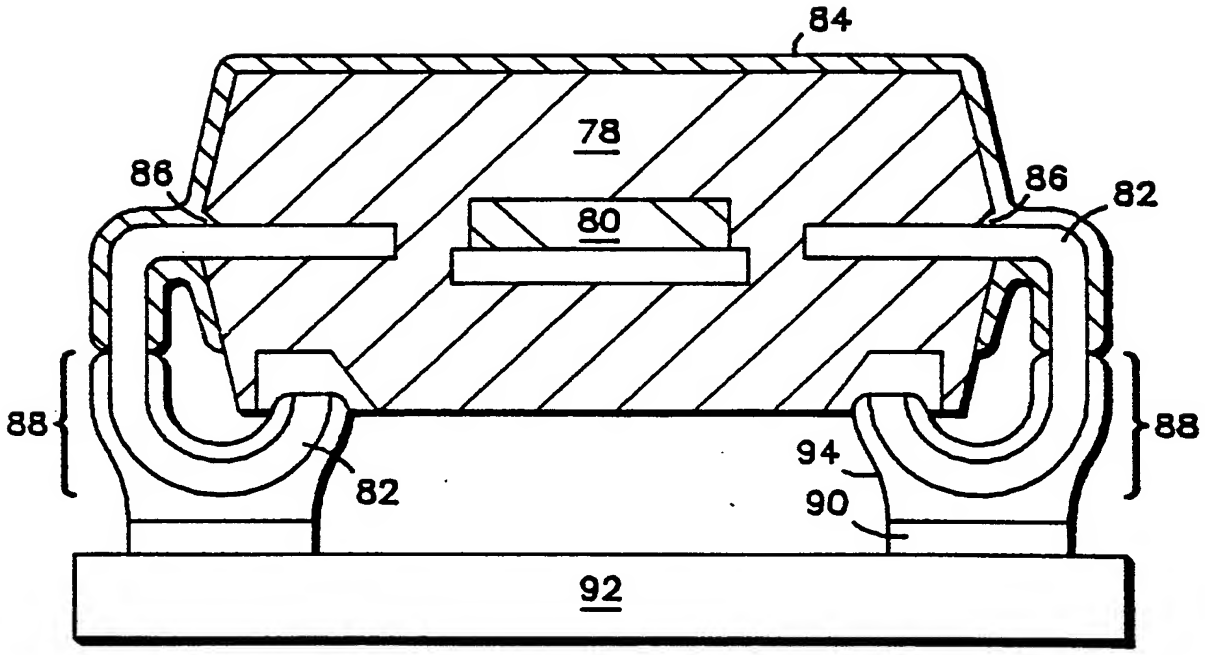
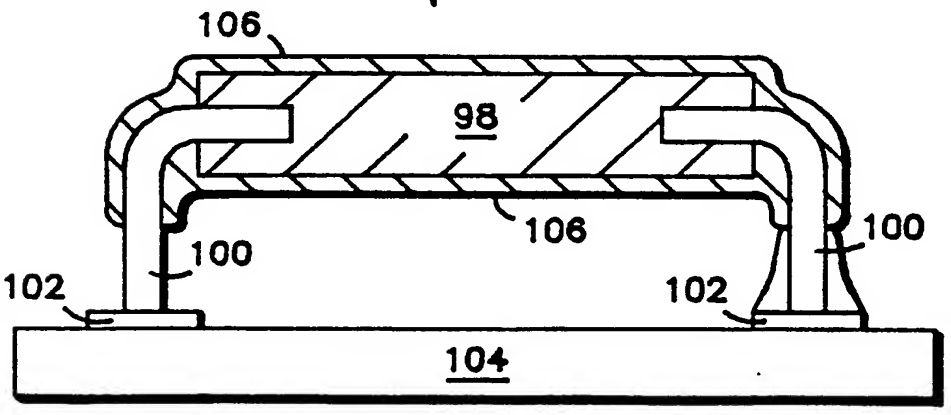


FIG. 6 76

FIG. 7



INTERNATIONAL SEARCH REPORT

International Application No PCT/US86/01883

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[4] H01L 23/28, 23/48, 29/44, 29/52, 29/54, 29/60
U.S. CL. 357/ 68, 70, 71, 72

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	357/ 68, 70, 71, 72

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4,147,889 (ANDREWS ET AL) 03 April 1979 see the entire reference	1-10
Y	US, A, 4,132,856 (HUTCHISON ET AL) 02 January 1979 see the entire reference	1-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [3]	Date of Mailing of this International Search Report [3]
17 November 1986	25 NOV 1986
International Searching Authority [1]	**Signature of Authorized Officer** [20]
ISA/US	E. Wojciehowicz/mh

Form PCT/ISA/210 (second sheet) (May 1986)